DESCRIPTION

WF4455RNC is a high performance OOK/ASK transmitter for the Remote Keyless Entry (RKE) systems. It consists of a power amplifier, one-shot circuit and phase-locked loop with internal voltage controlled oscillator and loop filter. The one-shot circuit control the phase-locked loop and power amplifier to have fast start-up time in operation.

FEATURES

- Highly integrated OOK/ASK transmitter
- High output power, 3 V /+11 dBm / 18mA
- Wide supply voltage, 1.8 V to 5.5 V operation range
- Low external component cost.
- PLL-based transmitter with frequency range from 250MHz to 450MHz
- On-chip one-shot circuit
- 60 dB RF on-off ratio for OOK/ASK modulation
- SOT23-6 Package

APPLICATIONS

- Keyless entry systems
- Remote control systems
- Garage door openers
- Alarm systems
- Security systems
- Wireless sensors

产品描述

WF4455RNC 是一款高性能 OOK/ASK 发射芯片.片内集成了一个功率放大器、One-short 电路、锁相环、压控振荡器和环路滤波器。 One-short 电路能快速控制环路锁相器和功放工作，以缩短发射启动时间

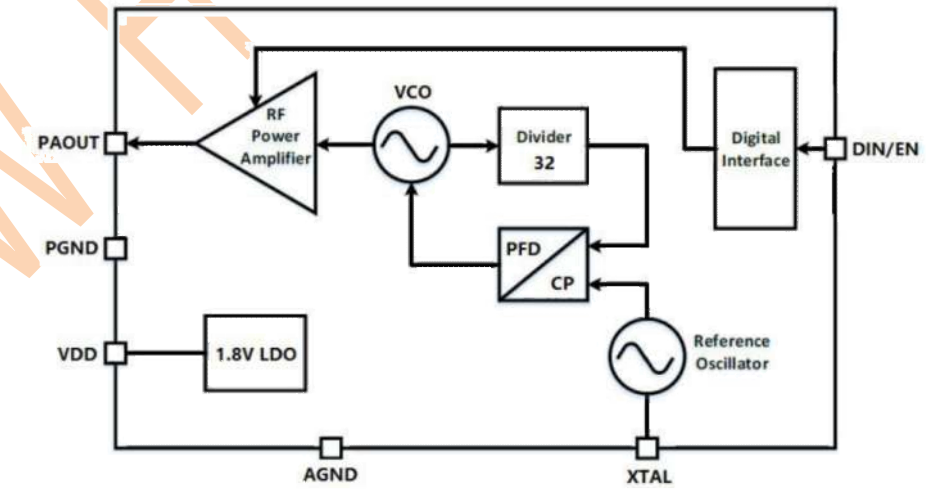
产品特性

- 高集成 OOK/ASK 发射芯片
- 大功率输出, 3 V /+11 dBm / 18 mA
- 宽工作电压, 1.8V to 5.5 V
- 极少的外围线路
- 工作频率范围 250MHz to 450MHz
- 片内 one-shot 电路
- 功率比高达 60 dB
- SOT23-6 封装

应用领域

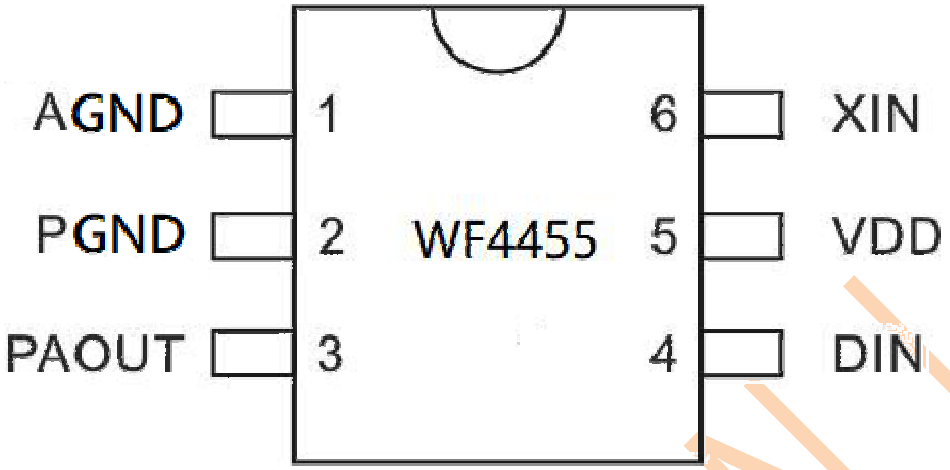
- RKE 无匙进入系统
- 无线遥控系统
- 门铃遥控
- 报警遥控
- Security systems
- 无线传感器

BLOCK DIAGRAM 框架图



WHOFDNIL

PIN CONFIGURATION 脚位定义



PIN DESCRIPTION 脚位说明

Pin Name	I/O	Description	Pin No.
AGND	O	Ground connection 地	1
PGND	G	Ground connection 地	2
PAOUT	O	Power amplifier output 射频输出	3
DIN	I	Data input 数据输入	4
VDD	P	Power supply 供电输入	5
XIN	I	Oscillator input 振荡输入	6

FUNCTION DESCRIPTION 功能描述

PA OUTPUT MATCHING

The PA output is an open-drain structure. Its output connects a large choke inductor to supply voltage and follows by a DC block capacitor. After the DC block capacitor, a C-L-C □-type matching network is used to tune with the antenna impedance. The inductor and capacitor values may be different from the suggestion value depending on PCB material, PCB thickness, ground configuration, and the layout traces length.

For the open-drain structure in PA, the HBM (Human Body Mode) and MM (Machine Mode) ESD strength is 4KV and 400V.

功放输出匹配

PA 输出为开漏结构。它的输出连接一个大的扼流圈电感来提供电压，然后串接一个隔直电容。在隔直电容之后，采用□型匹配网络与天线阻抗进行调谐。可以根据 PCB 材料、PCB 厚度、铺铜配置和走线长度，来微调电感和电容的值。

对于 PA 中的开漏结构，HBM(人体模式)和 MM(机器模式)的 ESD 强度分别为 4KV 和 400V。

WHOFDNL

REFERENCE OSCILLATOR

For a quartz crystal to oscillate in the specified frequency, it should work with vendor provided load capacitor value, called C_L . The load capacitor is about 12pF to 18pF in general. In WF4455, the colpitts crystal oscillator is used, and noneed external capacitors. The temperature coefficient of quartz crystal will cause the VCO output frequency drift in high/low temperature range.

With a fixed divided-by-32 PLL, the $f_{REFOSC} = f_{TX} / 32$. The following table list f_{REFOSC} for some common transmit frequencies

参考振荡器

为了使石英晶体在规定的频率内振荡，它应该与供应商提供的负载电容值(称为 CL)一起工作。负载电容一般在 12pF 到 18pF 之间。在 WF4455 中，使用了电容反馈型晶体振荡器，无需外部并联电容。石英晶体的温度系数会导致压控振荡器在高/低温度范围内的输出频率漂移。

用固定的 PLL 除以 32，则 $f_{REFOSC} = f_{TX} / 32$。下表列出了一些常见的传输频率的 f_{REFOSC}

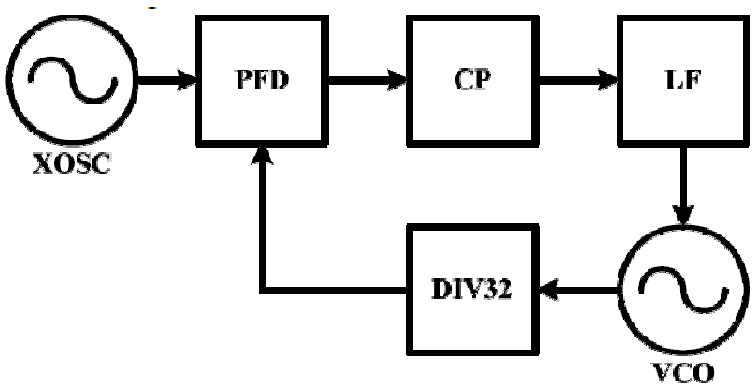
Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315 MHz	9.844 MHz
340 MHz	10.625 MHz
390 MHz	12.188 MHz
433.92 MHz	13.56 MHz

PHASE-LOCKED LOOP (PLL)

The WF4455 own a fixed divided-by-32 PLL to generate the transmitter signal. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous ÷ 32 divider, charge pump, loop filter and phase-frequency detector (PFD). All these circuits are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an approximately 180 KHz bandwidth, and is used to control the VCO. A frequency divider placed after the VCO and it will feedback the divided signal to PFD. In the final the VCO will get locked to reference signal as $f_{VCO} = f_{REFOSC} * 32$. The block diagram below shows the basic elements of the PLL.The PLL chain circuit is supplied by internal voltage regulator to ease the PA pulling and crystal spur issue

锁相环

WF4455 拥有一个固定的 32 分锁相环来产生发射信号。该锁相环由压控振荡器(VCO)、晶体振荡器、异步分频器、电荷泵、环路滤波器和相频检波器(PFD)组成。所有这些电路都集成在芯片上。PFD 比较两个信号并产生与输入相位之间的差成比例的误差信号。误差信号通过一个带宽约为 180khz 的环路滤波器，并用于控制 VCO。位于压控振荡器后的分频器，它将分频信号反馈给 PFD。在最后，VCO 将被锁定为参考信号 $f_{VCO} = f_{REFOSC} * 32$。下面的框图显示了锁相环的基本元素。锁相环链电路由内部稳压器提供，以消除 PA 拉动和晶体激射问题



HOEDN-L

ONE-SHOT CIRCUIT AND POWER-DOWN CONTROL

During the signal transmission, the crystal oscillator start-up time will limit its wake-up time to work. A one-shoot circuit is used to solve this problem by turning on/off the power amplifier and PLL circuit separately.

When apply “HIGH” to DIN, will enable the PLL chain and PA. When applied “LOW” to DIN, the PA will be turn-off immediately, and the PLL chain will be turn-off after one-shot period about 50ms.

To calculate the re-triggerable one-shot delay time, it can be counted as 688128 / f_{REFOSC} . For f_{REFOSC} = 9.844MHz and 13.56MHz, the delay time is about 70ms and 50ms.

ANTENNA DESIGN AND PCB LAYOUT CONSIDERATION

For a λ/4 dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L \approx \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a λ/4 antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to λ/8, λ/16, etc. without degrading the input return loss. Usually, when designing a λ/4 dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where “c” is the speed of light (3 x10^{10} cm/s)

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the GND pins. Grounding the metal case of quartz crystal and isolate the XIN/XOUT trace to other can suppress the crystal spur signal over PA output.

ONE-SHOT 电路和断电控制

在信号传输过程中，晶体振荡器的启动时间将限制晶体振荡器的唤醒时间。为了解决这一问题，我们采用了 one-shot 电路，它直接打开/关闭功率放大器和锁相环电路。

当“高电平”加到 DIN，将启用锁相环和 PA。当应用“低电平”加到 DIN 时，PA 将立即关闭，锁相环将在约 50ms 后关闭。

计算可重新触发的延迟时间，可用 688128 / f_{REFOSC} 来计算。对于 f_{REFOSC} = 9.844MHz 和 13.56MHz，延迟时间分别约为 70ms 和 50ms。

天线设计和 PCB 布局

对于 1/4 波长偶极子天线和工作频率，f (MHz)，需要的天线长度 L (cm)，可以使用公式计算

$$L \approx \frac{7132}{f}$$

例如，如果频率是 315 MHz，那么 λ/4 天线的长度是 22.6 cm。如果计算的天线长度对于应用来说太长了，那么它可以减少到 λ/8，λ/16 等，而不降低输入回波损耗。通常，在设计 λ/4 偶极子天线时，使用单根导电导线(直径约 0.8 mm ~ 1.6 mm)比使用多芯导线更好。

如果在 PCB 板上打印天线，请确保 PCB 板背面天线下方没有器件，也没有接地面。对于一个 FR4 PCB(ε_r = 4.7)和一个 30 mil 的条宽，天线的长度 L (in cm)计算

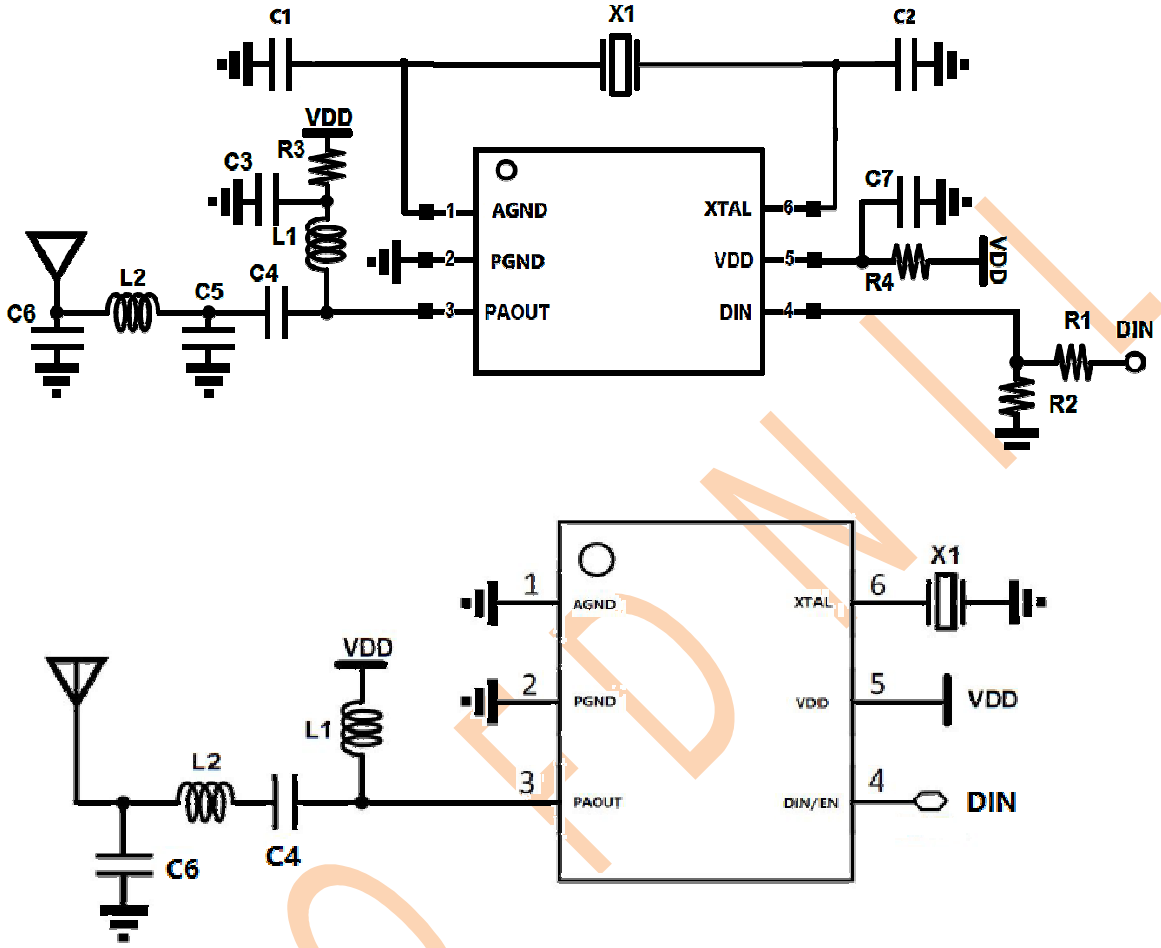
$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where “c” is the speed of light (3 x10^{10} cm/s)

正确的 PCB 布局对于获得良好的射频性能至关重要。至少，强烈建议使用两层 PCB，以便其中一层可以包含连续的接地面。上层与底层之间的地平面区域应设置大量过孔。

还必须仔细考虑 PCB 一级的供电和接地。较大的接地平面应尽可能地靠近所有的 GND 引脚。将石英晶体的金属外壳接地和隔离 XIN/XOUT 走线，可以抑制晶体脉冲信号的输出。

FEEDNIL

APPLICATION CIRCUIT 应用电路



BILL OF MATERIALS 物料清单

Part	Value		Unit
	315MHz	433.92MHz	
X1	9.844M	13.56M	Hz
R1	0	0	Ω
R2	NC	NC	Ω
R3	0	0	Ω
R4	0	0	Ω
C1	0	0	Ω
C2	NC	NC	F
C3	1μ/NC	1μ/NC	F
C4	220p	220p	F
C5	NC	NC	F
C6	18p	10p	F
C7	2.2μ/NC	2.2μ/NC	F
L1	180n	180n	H
L2	33n	27n	H

1. L2/CC/C6 value will depend on PCB layout.
2. C3,C7 are for EMC.

FOR ONLY

ABSOLUTE MAXIMUM RATINGS 极限参数

(V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	5	V
I/O Voltage	$V_{I/O}$	-0.3	5	V
Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature Range	T_{STG}	-55	+125	°C

RECOMMENDED OPERATING CONDITIONS

推荐工作参数

(VGND=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	5.5	V
Operating Temperature Range	T_A	-40	+85	°C

ELECTRICAL CHARACTERISTICS 电气参数

Nominal conditions: V_{DD} = 3.0 V, V_{SS} = 0 V, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD}		1.8	3.0	5.5	V
Operating Current (Note)	I_{DD}	DIN=High(CW mode); P_{OUT} =12dBm, f_{RF} = 315MHz		17		mA
		DIN=High(CW mode); P_{OUT} =12dBm, f_{RF} = 434MHz		18		mA
Standby Current	$I_{standby}$	DIN=Low; T_{DELAY}>50ms			1	□A
RF□						
Frequency Range	f_{RF}		250		450	MHz
Power Amplifier Output Power (Note)	P_{out}	f_{RF} = 315MHz		11		dBm
		f_{RF} = 434MHz		10		dBm
RF Power On / Off Ratio	P_{EXT}			60		dB
Phase Noise	P_{NOISE}	315MHz, 10KHz offset		-75		dBc/Hz
Harmonics (Note)	P_{HARM}	2x/3x f_{RF}		-40		dBc
Crystal Spur	P_{SPUR}	f_{RF} = 315MHz		-50		dBc
		f_{RF} = 434MHz		-50		dBc
Data Input and One-shot						
Data Rate	D_{RATE}		0.5	2	20	Kbps
Crystal Oscillator Start-up Time	T_{ON}	C_L not connected		1		ms
One-shot Delay Time	T_{DELAY}		50			ms

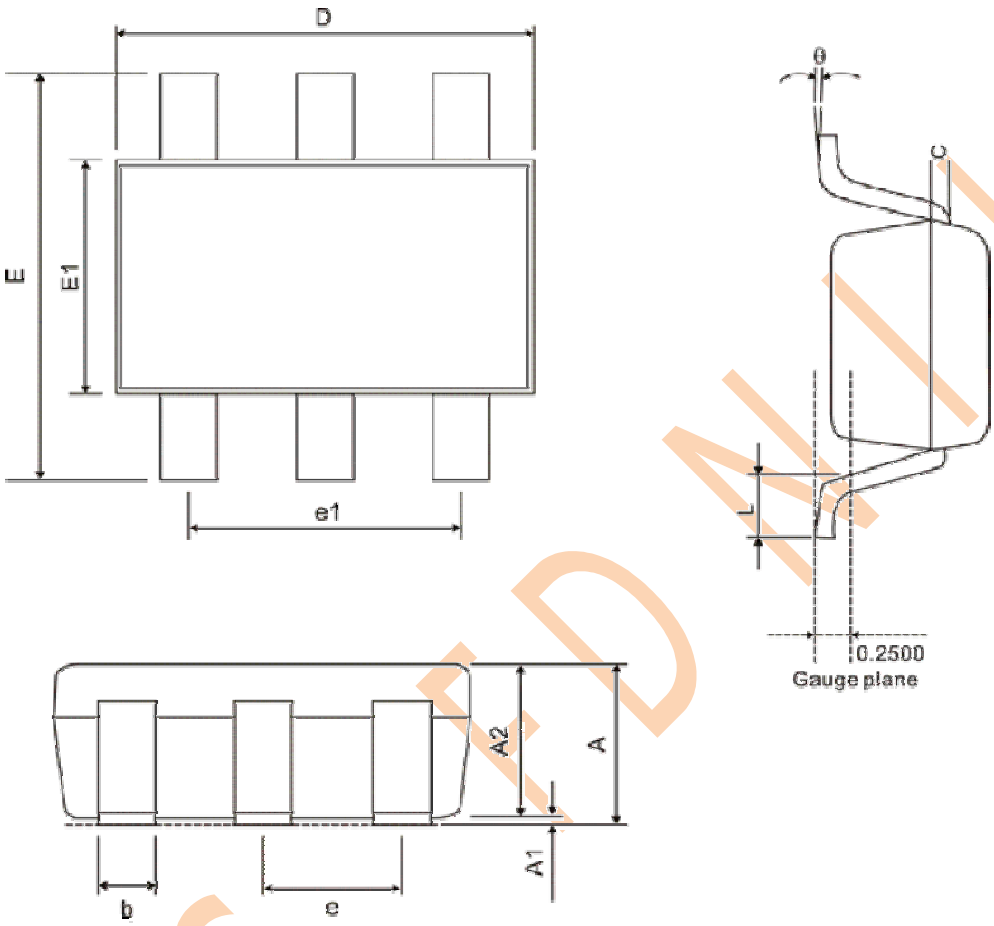
Note: Depend on power amplifier output matching

ORDER INFORMATION 购买信息

Part Number 物料编号	Package 封装类型	Package Option 包装方式	MPQ 最小包装数量
WF4455TD ST6 RNC	6 Pins, SOT23	Tape&Reel 卷装	3000 PCS

PACKAGE INFORMATION 封装信息

6 Pins, SOT23-6



Symbol	Min.	Nom.	Max
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
c	0.080	0.130	0.200
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
θ	0°	-	8°
L	0.30	0.45	0.60

All dimensions are in millimeter

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